We claim:

1. A method for forming a flash memory structure, comprising:

providing a semiconductor substrate with isolation structures, a first dielectric layer, and a first polysilicon layer on said first dielectric layer;

forming an inter-polysilicon dielectric layer on said first polysilicon layer;

forming a second polysilicon layer on said inter-polysilicon layer;

forming a hardmask layer on said second polysilicon layer;

forming a patterned photoresist film on said hardmask layer; and

etching said hardmask layer, said second polysilicon layer, and said inter-polysilicon dielectric layer with a multi-step etch process wherein said multi-step etch process removes said patterned photoresist layer.

2. The method of claim 1 wherein said inter-polysilicon dielectric layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

3. The method of claim 1 wherein said inter-polysilicon dielectric layer comprises any number of alternating layers of silicon oxide and silicon nitride.

4. The method of claim 1 wherein said hardmask comprises a silicon nitride layer.

5. A method to form a self-aligned source in a memory cell, comprising:

providing a semiconductor substrate with a memory structure comprising a first dielectric layer, a first polysilicon layer on said dielectric layer, an inter-polysilicon dielectric layer on said first polysilicon layer, a second polysilicon layer on said inter-polysilicon dielectric layer, and a hardmask layer on said second polysilicon layer;

performing a self-aligned source etch process;

forming a cap layer on said memory structure;

performing an anisotropic cap layer etch to form sidewall structures on said memory structure; and

removing said hardmask layer using a hardmask etch process.

6. The method of claim 5 wherein said hardmask layer comprises a silicon oxide layer and a silicon nitride layer.

7. The method of claim 6 wherein said self-aligned source etch comprises a dry silicon oxide etch.

8. The method of claim 6 wherein said cap layer comprises silicon oxide.

9. The method of claim 8 wherein said removing said hardmask layer comprises using a hot phosphoric etch process.

10. A method of forming a memory cell structure, comprising:

providing a semiconductor substrate with isolation structures, a first dielectric layer, and a first polysilicon layer on said first dielectric layer;

forming an inter-polysilicon dielectric layer on said first polysilicon layer;

forming a second polysilicon layer on said inter-polysilicon layer;

forming a hardmask layer on said second polysilicon layer;

forming a patterned photoresist film on said hardmask layer;

etching said hardmask layer, said second polysilicon layer, and said inter-polysilicon dielectric layer with a multi-step etch process to form a memory structure wherein said multi-step etch process removes said patterned photoresist layer;

performing a self-aligned source etch process;

forming a cap layer on said memory structure;

performing an anisotropic cap layer etch to form sidewall structures on said memory structure; and

removing said hardmask layer using a hardmask etch process.

11. The method of claim 10 wherein said inter-polysilicon dielectric layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

12. The method of claim 10 wherein said inter-polysilicon dielectric layer comprises any number of alternating layers of silicon oxide and silicon nitride.

13. The method of claim 10 wherein said hardmask comprises a silicon nitride layer.

14. The method of claim 10 wherein said self-aligned source etch comprises a dry silicon oxide etch.

15. The method of claim 13 wherein said cap layer comprises silicon oxide.

16. The method of claim 15 wherein said removing said hardmask layer comprises using a hot phosphoric etch process.